IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application	)	
	)	
ODA et al.	)	
	)	
Application Number: To be Assigned	)	
	)	**Art Unit 2811**
Filed: Concurrently herewith	)	
	)	
For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD	)	
	)	
	)	
Attorney Docket No. HITA.0474	)	

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

The above-referenced application is a Divisional of U.S. Serial No. 09/824,225 filed April 3, 2001. It includes the same disclosure as U.S. patent application Serial No. 09/824,225.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application, pursuant to 37 CFR § 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

This Information Disclosure Statement is submitted with the above-captioned U.S. Divisional application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,

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December 18, 2003

Form PTO 1449 U.S. Department of commerce Patent and Trademark Office Information Disclosure Statement by Applicant	ATTY. DOCKET NUMBER **HITA.0474**	SERIAL NUMBER **To be assigned**
	APPLICANT **ODA et al.**	
	FILING DATE **Concurrently herewith**	GROUP

U.S. Patent Documents

Examiner Initial		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	**	6,350,993	02/26/2002	Chu et al.	257/192		03-12-1999

Foreign Patent Documents

Examiner Initial		DOCUMENT NUMBER	FILING DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	No
	**	0307850	09-13-1988	EPO			Abstract	X

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

	*	Konig et al., "p-Type SiGe Channel Modulation Doped Field-Effect Transistors with Post-Evaporation Patterned Submicrometre Schottky Gates," IEEE Electronics Letters, Vol. 29, No. 5, March 4, 1993, pp. 486-688
	*	Konig et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters, Vol. 14, No. 4, April 1993, pp. 205-207
	*	Konig et al., "Enhancement Mode n-Channel Si/SiGe MODFET with High Intrinsic Transconductance," IEE Electronics Letters, Vol. 28, No. 2, January 16, 1992, pp. 160-162
	*	Sadek et al., "Design on Si/SIGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEEE Transactions on Electron Devices, Vol. 43, No. 8, August 1996, pp. 1224-1232

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant

PTO 1449

*** Cited by Applicant in Parent**
**** Cited by Examiner in Parent**